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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/957,004	09/19/2001	Kollin Tierling	IMM135	2443

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EXAMINER	
NGUYEN, NAM V	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/957,004	Applicant(s) TIERLING, KOLLIN	
	Examiner Nam V Nguyen	Art Unit 2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Tierling for a "circuit and method for a switch matrix and switch sensing" filed September 19, 2001 has been examined.

Claims 1-26 are pending.

Information Disclosure Statement

The information disclosure form (PTO-1449) was filed on September 27, 2002 is not in the application folder. Therefore, examiner suggests to re-submit a copy of the PTO-1449 again for consideration by the examiner.

Drawings

This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

The drawings are objected to under 37 CFR 1.83(a) because they fail to label boxes (222) in Figure 7 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "processor" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: the processor 20 discloses in page 6 line 8 and line 17 in the specification, however, in the Figures 4-7 are not labeled and have refer to the same element with switch matrix 20 in Figure 3. Consistent reference is required.

The disclosure is objected to because of the following informalities: the resistor R6 discloses in page 6 line 9 in the specification, however, in the Figures 4-7 are not labeled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 6-7, 10-15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US# 5,760,714) in view of Houston et al. (US# 3,921,140).

Referring to claims 1-2, Zimmerman discloses a switch matrix circuit (100) (i.e. an electronic device) (column 1 line 22 to 47; see Figure 1) comprising:

A plurality of switches (70) (i.e. a keypad matrix) organized in a row ((15) and column (10) configuration (column 2 lines 46 to 61; see Figure 1); and

A current sensing circuit (19 and 16) coupled to the plurality of switches (70) (column 2 lines 46 to 56; see Figure 1), the current sensing circuit including at least one resistor (19) (i.e. a pull up resistor) per column (10, 20, 30 or 40) of the plurality of switches (70) (column 2 lines 57 to column 3 line 9), wherein current amplified by the falling/rising edge triggered interrupt and converted by the at least one resistor (19) in a column (10) is sensed as a logic level indicative of a switch (11) status within the column (10) for a selected row (15) (column 3 lines 22 to 59; see Figure 3).

However, Zimmerman did not explicitly disclose the current sensing circuit including a transistor.

In the same field of endeavor of switch scanning matrix, Houston et al. teach that the current sensing circuit (5) (i.e. a horizontal isolation transistor unit) including a bipolar transistor (85) (column 2 lines 36 to 64; see Figures 1 and 5) in order to detect the level of the output voltage when a switch is closed.

One of ordinary skilled in the art recognizes using a transistor in a horizontal isolation transistor unit to detect voltage of Houston et al. in all the column line interrupts of a sequentially

scans for output signal of Zimmerman because Zimmerman suggests it is desired to provide that using a rising/falling edge triggered interrupt component in a sensing circuit to determine which key, if any, was validly pressed (column 2 line 57 to column 3 line 22; see Figures 1-3) and Houston et al. teach that using a transistor in a horizontal isolation transistor unit to detect the changing voltage signal level of a switch when the switch is pressed (column 2 lines 19 to 64; see Figures 1 and 5) in order to have a successful and reliable detecting the level of the output voltage of each switch. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use a transistor in a horizontal isolation transistor unit to detect voltage of Houston et al. in all the column line interrupts of a sequentially scans for output signal of Zimmerman with the motivation for doing so would have been to provide a reliable and valid of sensing a switch status when pressed.

Referring to claim 6, Zimmerman in view of Houston et al. disclose a switch matrix circuit of claim 1, Zimmerman discloses wherein a processor (99) (i.e. a microcontroller) senses the switch status (column 2 line 54 to 66; column 3 lines 33 to 64; see Figures 1-3).

Referring to claims 7 and 13, Zimmerman in view of Houston et al. disclose a switch matrix circuit and method of claim 1, the claims 7 and 13 differ from claim 1 is that the claims 7 and 13 requires the limitation of claim 6 already addressed above and Zimmerman discloses all the limitation to the extent as claimed with respect to claim 6 above and therefore claims 7 and 13 is also rejected as being obvious for the same reasons given with respect to claim 1.

Referring to claims 10-12, 14-15 and 18, Zimmerman in view of Houston et al. disclose a switch matrix circuit of claims 7 and 13, the claims 10-12, 14-15 and 18 same in that the claim 1 already addressed above therefore claims 10-12, 14-15 and 18 are also rejected for the same reasons given with respect to claim 1.

Claims 3-5 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US# 5,760,714) in view of Houston et al. (US# 3,921,140) and in further view of Hastreiter (US# 4,667,181).

Referring to claims 3-5 and 19-21, Zimmerman in view of Houston et al. disclose a switch matrix circuit of claim 1, however, Zimmerman in view of Houston et al. did not explicitly disclose a the row and column configuration further comprises an off-diagonal configuration having one switch per row and column intersection in all but one intersection per row.

In the same field of endeavor of scanning switch matrix, Hastreiter discloses a row (11) (i.e. a first plurality of conductors) and column (12) (i.e. a second plurality of conductors) configuration (column 3 lines 30 to 48; see Figure 1) further comprises an off-diagonal configuration having one switch (13) per row (11) and column (12) intersection in all but one intersection per row (column 3 lines 49 to 59; see Figure 1) in order to connect directly to a data processor which has bi-directional input/output ports.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to recognize to use a switch of a matrix of keyboard conductors that located at each

intersection of the conductors except along one diagonal group of intersections of Hastreiter in keypad switch matrix of Zimmerman in view Houston et al. of because having a switch that located at each intersection of the conductors except along one diagonal group of intersections would able to connect directly to a data processor which has bi-directional input/output ports that has been shown to be desirable in the keypad switch matrix circuit of Zimmerman in view of Houston et al.

Referring to claim 21, Zimmerman in view of Houston et al. and Hastreiter disclose a switch matrix circuit of claim 19, Houston et al. disclose a diode (76) and resistor (77) circuit for each scan line (column 1 line 53 to 62; see Figures 3-5).

Claims 8-9 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US# 5,760,714) in view of Houston et al. (US# 3,921,140) as applied to claims 7 and 13 and in further view of Valdenaire (US# 5,677,687).

Referring to claims 8 and 16, Zimmerman in view of Houston et al. disclose a switch matrix circuit and method of claims 7 and 13, however, Zimmerman in view of Houston et al. did not explicitly disclose wherein the plurality of scan lines further comprise a plurality of bi-directional scan lines wherein a single scan line provides both row selection and column sensing capabilities.

In the same field of endeavor of scanning switch matrix, Valdenaire discloses a plurality of bi-directional scan lines (C1 to C5 and R1 to R5) wherein a single scan line (C1) provides

both row selection and column sensing capabilities (column 3 lines 7 to 25; see Figures 1-4) in order to take full advantage of the switch matrix circuit input and output.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to recognize to use a plurality of bi-directional input and output circuit of Valdenaire in input and output of the microprocessor that connect to the switch matrix circuit of Zimmerman in view of Houston et al. because bi-directional input or output circuit result would improve the efficiently and more compact that has been shown to be desirable in the interrupt-driven keypad scanning switch matrix circuit of Zimmerman in view of Houston et al.

Referring to claims 9 and 17, Zimmerman in view of Houston et al. and in further view of Valdenaire disclose a switch matrix circuit of claims 8 and 16, Zimmerman discloses wherein the organization of the plurality of switches (70) further comprise an off-diagonal organization to support the bi-directional scan lines (10 and 15) (column 2 lines 46 to 56; see Figures 1-4).

Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US# 5,760,714) in view of Houston et al. (US# 3,921,140) and in further view of Feucht et al. (US# 3,689,889).

Referring to claims 23-26, Zimmerman in view of Houston et al. disclose a circuit for more efficient switch selection sensing, to the extent as claimed with respect to claim 1 above, however, Zimmerman in view of Houston et al. did not explicitly disclose a circuit further including:

A plurality of resistors, each of the resistors electrically coupled in series with an associated one of the plurality of switches.

In the same field of endeavor of scanning switch matrix, Feucht et al. disclose a circuit further including: a plurality of resistors (R11), each of the resistors (R11) electrically coupled in series with an associated one of the plurality of switches (X11) (column 2 lines 56 to column 3 line 6; column 4 lines 3 to 38; see Figures 1-4) in order to protect against false closure of threshold value switches.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to recognize to use each resistor in series with an associated one of the plurality of switches of Feucht et al. in keypad switch matrix of Zimmerman in view Houston et al. of because using a resistor in series with a switch would improve the protection against false closure of threshold value switches that has been shown to be desirable in the keypad switch matrix circuit of Zimmerman in view of Houston et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsuda (US# 5,151,554) discloses a high speed switch scanning apparatus.

Kinerk et al. (US# 5,486,824) disclose a data processor with a hardware keyscan circuit, hardware keyscan circuit, and method therefor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam V Nguyen whose telephone number is 703-305-3867. The examiner can normally be reached on Mon-Fri, 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on 703-305-4704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Nam Nguyen
May 7, 2004

MICHAEL HORABIK
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